

FIG. 2

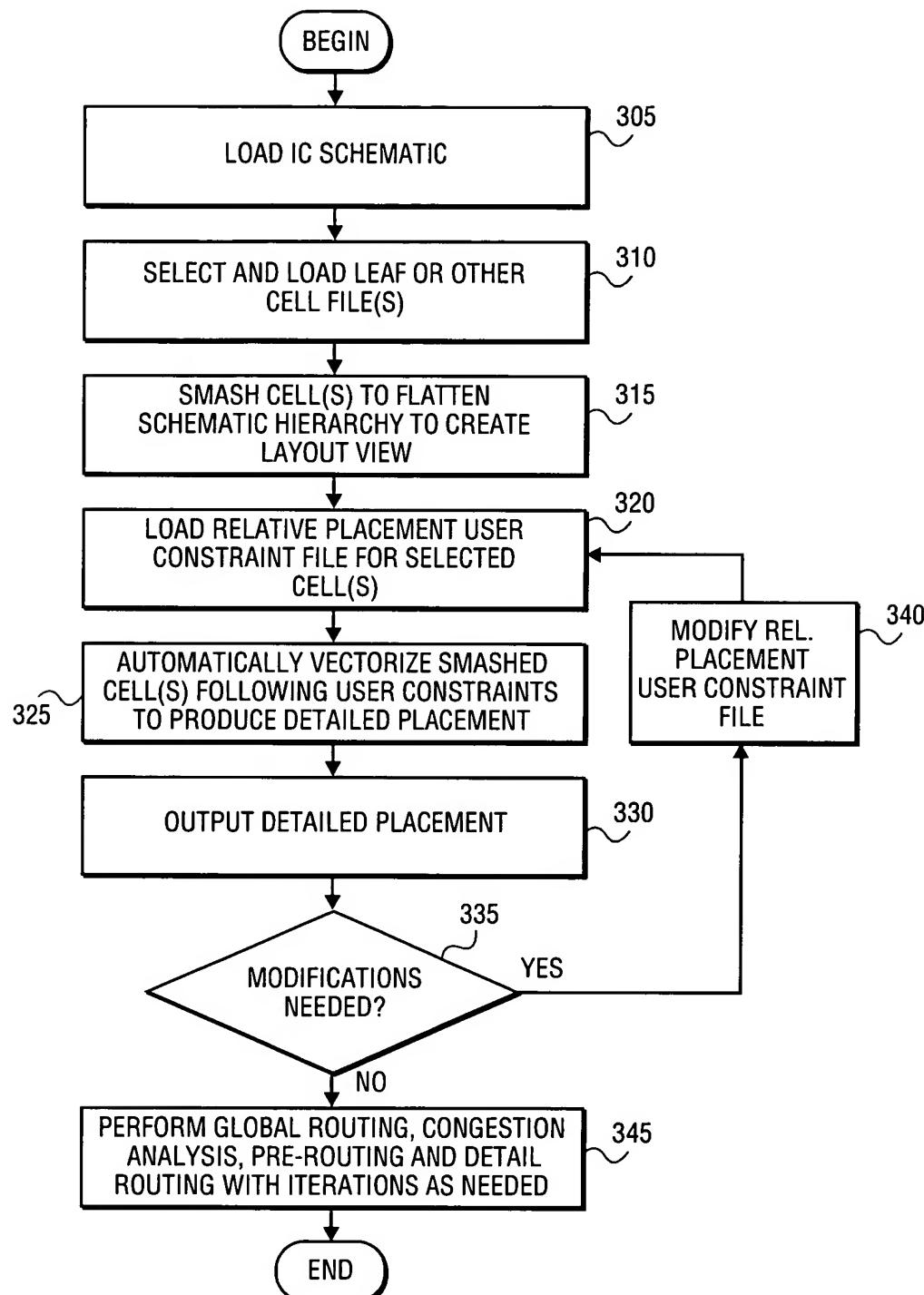


FIG. 3



SPECIFICATION	IMPLICATION
(1) V1 = vector{a(0:9)}	a[0] a[2] a[4] a[6] a[8] a[9]
(2) V2 = vector (stride 2) {b(0:4)}	b[1] b[3]
(3) V3 = vector{c(0,5,6:8) d(0:3:2)}	c[0] c[5] c[6] c[7] c[8] d[0] d[2]
(4) V4 = vector{skip(2) j(0:1)}	j[0] j[1]
(5) V5 = step{interleave{v3 v4} i[(0)]}	c[0] c[5] c[6] j[0] c[7] j[1] c[8] d[0] d[2] i[0]
(6) V6 = merge{V1 V2}	
(7) V7 = interleave {vector{Tall(0:4)} merge{vector{x(0:4)} vector{y(0:4)}}	
(8) hg = Vabut{V6 step{v7 zzinst}}	
	0 1 2 Bits ---> 6 ,...

FIG. 4

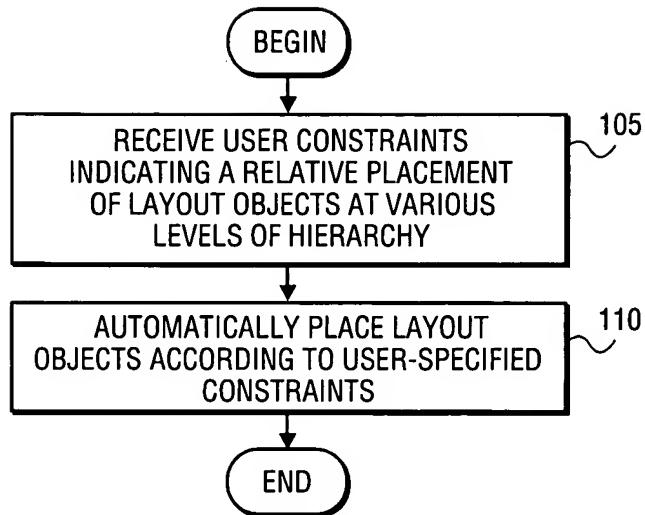


FIG. 1

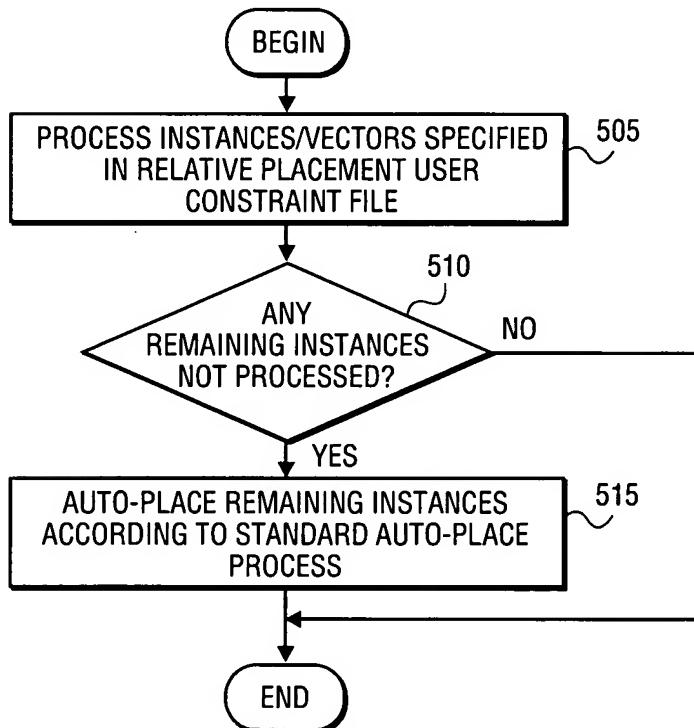


FIG. 5

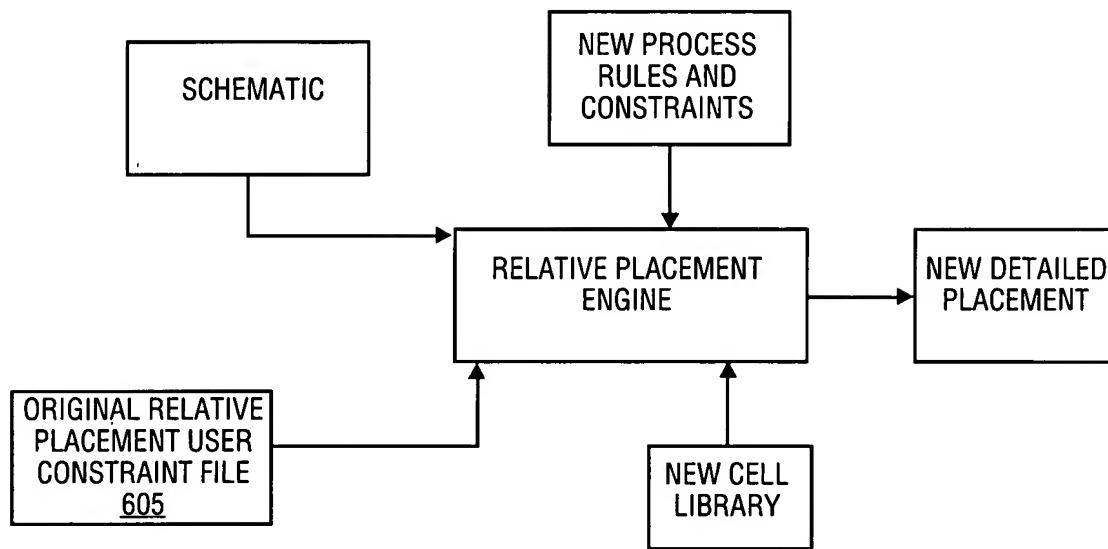


FIG. 6

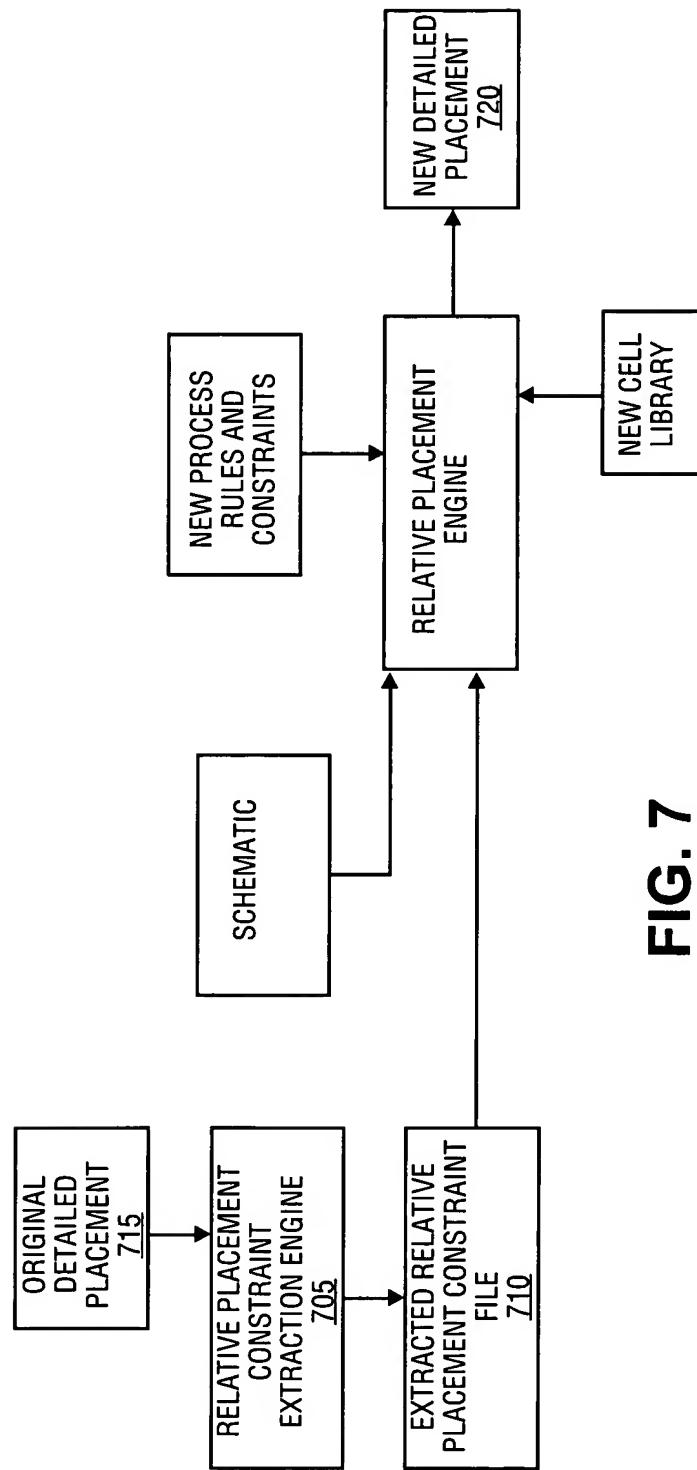


FIG. 7